IN THE SPECIFICAITON

Please amend the specification as follows:

The paragraph beginning at page 2, line 25 is amended as follows:

B1

Dadda's multiplier uses the scheme shown in ~~on~~ figure 14. If inputs have 8 bits then 64 parallel AND gates generate an array shown in figure 15. The AND gate sign ^ is omitted for clarity so that Ai^Bj becomes AiBj. The rest of figure 15 illustrates array reduction that involves full adders (FA) and half adders (HA). Bits from the same column are added by half adders or full adders. Some groups of bits fed into a full adder are in rectangles. Some groups of bits fed into a half adder are in ovals. The result of array reduction is just two binary numbers to be added at the last step. One adds these two numbers by one of fast addition schemes, for instance, conditional adder or carry-look-ahead adder.

The paragraph beginning at page 3, line 4 is amended as follows:

B2

In accordance with the first aspect the present invention provides a parallel counter which is based on algebraic properties of symmetric functions. ~~Each of the plurality of binary output bits is generated as a symmetric function of a plurality of binary input bits to a~~ A plurality of ~~the~~ binary output bits are ~~each~~ generated as a symmetric function of a plurality of ~~a binary~~ input bits.

The paragraph beginning at page 15, line 10 is amended as follows:

B3

Although in this embodiment the [addition] multiplication of two 8 bit numbers has been illustrated, the invention is applicable to any N bit binary number [addition] multiplication. For example for 16 bit [addition] multiplication, the array reduction will reduce the middle column height from 16 to 15 thus allowing two seven bit full adders to be used for the first layer to generate two 3 bit outputs and the left over input can be used with the other two 3 outputs as an

B3

input to a further seven input full adder thus allowing the addition of the 16 bits in only two layers.